WHAT IS CLAIMED IS:

1. A power control circuit for controlling power provided across a power device, comprising:

sensing circuitry for providing a sense result signal in response to a sense input signal, the sense input signal including information received through a gating device connected between the sensing circuitry and the power device; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry for preventing the sense input signal from including spurious information received from the gating device.

2. The circuit of claim 1 in which the gating device provides spurious negative spikes, the correction circuitry preventing negative spikes in the sense input signal.

3. The circuit of claim 2 in which the gating device is a diode and the power device is a field effect transistor (FET); the diode being turned on when the FET is on and being turned off when the FET is off; the correction circuitry preventing negative spikes in the sense input signal except when the FET is on.

4. The circuit of claim 1 in which the sensing circuitry includes a comparator for comparing signals received at first and second inputs and for providing the sense result signal at an output, the first input receiving the sense input signal and the second input receiving a reference signal; the correction circuitry receiving the sense result signal from the comparator's output and preventing

negative spikes in the sense input signal when the sense result signal indicates that the sense input signal is greater than the reference signal.

5. The circuit of claim 4, further comprising an integrated circuit that includes the sensing circuitry and the correction circuitry; the integrated circuit further including:

a sensing node for connecting to the power device through the gating device; and

a voltage source connected to provide the reference signal to the comparator's second input, a first resistance between a supply voltage and the sensing node, a second resistance between the sensing node and the comparator's first input, and a third resistance between the comparator's first input and ground; the voltage source and the first, second, and third resistances having values such that the sense input signal drops below the reference signal if the gating device turns on; the correction circuitry including a switchable impedance parallel to the first resistance, the switchable impedance being turned on only when the sense result signal indicates that the sense input signal is greater than the reference signal.

6. The circuit of claim 1, further comprising an integrated circuit that includes the sensing circuitry and the correction circuitry; the integrated circuit further including a sensing node for connecting to the power device through the gating device; the correction circuitry including a switchable impedance between a power supply and the sensing node and switching circuitry for switching the impedance on and off in response to a device state signal indicating whether the power device is on or off, the switchable impedance being turned on except when the device state signal indicates that the power device is on.

7. The circuit of claim 6 in which the correction circuitry further includes a comparator for comparing signals received at first and second inputs and for providing the device state signal at its output, the first input receiving a voltage at the sensing node and the second input receiving a reference voltage; the comparator's output being connected for turning the switchable impedance on only when the device state signal indicates that the sensing node voltage is greater than the reference voltage.

8. The circuit of claim 6 in which the sensing circuitry provides the device state signal to the switching circuitry.

9. An integrated power control circuit for controlling power provided across a power device, comprising:

a sensing node for connecting to the power device through a gating device;

sensing circuitry for providing a sense result signal in response to a sense input signal, the sense input signal including information received at the sensing node through the gating device; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry for preventing the sense input signal from including spurious information received at the sensing node from the gating device.

10. The circuit of claim 9 in which the sensing node is a desat/voltage feedback pin and in which the gating device provides spurious negative spikes to the sensing node, the correction circuitry being connected to the sensing node to prevent negative spikes in the sense input signal.

11. The circuit of claim 10 in which the gating device is a diode and the power device is a field effect transistor (FET); the diode being turned on when the FET is on and being turned off when the FET is off; the correction circuitry preventing negative spikes in the sense input signal except when the FET is on.

12. The circuit of claim 9 in which the sensing circuitry includes a comparator for comparing signals received at first and second inputs and for providing the sense result signal at an output, the first input receiving the sense input signal and the second input receiving a reference signal; the correction circuitry receiving the sense result signal from the comparator's output and preventing negative spikes in the sense input signal only when the sense result signal indicates that the sense input signal is greater than the reference signal.

13. The circuit of claim 12, further comprising a voltage source connected to provide the reference signal to the comparator's second input, a first resistance between a supply voltage and the sensing node, a second resistance between the sensing node and the comparator's first input, and a third resistance between the comparator's first input and ground; the capacitance and the first, second, and third resistances having values such that the sense input signal drops below the reference signal if the gating device turns on; the correction circuitry including a switchable impedance path parallel to the first resistance, the switchable impedance path being turned on only when the sense result signal indicates that the sense input signal is greater than the reference signal.

14. The circuit of claim 9 in which the correction circuitry includes a switchable impedance between a power supply and the sensing node and switching circuitry for switching the impedance on and off in response to a device

state signal indicating whether the power device is on or off, the switchable impedance being turned on except when the device state signal indicates that the power device is on.

15. The circuit of claim 14 in which the correction circuitry further includes a comparator for comparing signals received at first and second inputs and for providing the device state signal at its output, the first input receiving a voltage at the sensing node and the second input receiving a reference voltage; the comparison result signal being connected for turning the switchable impedance on only when the device state signal indicates that the sensing node voltage is greater than the reference voltage.

16. The circuit of claim 14 in which the sensing circuitry provides the device state signal to the switching circuitry.

17. An integrated power control circuit for controlling power provided across high and low side power devices connected in a half bridge, the circuit comprising high side circuitry for controlling the high side power device and low side circuitry for controlling the low side power device;

the high side circuitry comprising:

a first sensing node for connecting to the high side power device through a first gating device;

first sensing circuitry for providing a first sense result signal in response to a first sense input signal, the first sense input signal including information received at the first sensing node through the first gating device; the first sense result signal including information derived from the first sense input signal about operation of the first power device; and

first correction circuitry for preventing the first sense input signal from including spurious information received at the first sensing node from the first gating device; and

the low side circuitry comprising:

a second sensing node for connecting to the low side power device through a second gating device;

second sensing circuitry for providing a second sense result signal in response to a second sense input signal, the second sense input signal including information received at the second sensing node through the second gating device; the second sense result signal including information derived from the second sense input signal about operation of the second power device; and

second correction circuitry for preventing the second sense input signal from including spurious information received at the second sensing node from the second gating device.